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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,547	04/19/2004	Lukas P.P.P. van Ginneken	SYNP 1006-0	3884

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SYNOPSYS, INC. C/O HAYNES BEFFEL & WOLFELD LLP
P.O. BOX 366
HALF MOON BAY, CA 94019

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
01/15/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,547	VAN GINNEKEN, LUKAS P.P.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *03 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 and 4-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 4-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/3/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Petition decision under 1.48(a)*.

DETAILED ACTION

1. This office action is in response to application 10/828,547 and response filed on 11/3/2008. Claims 2 and 4-15 remain pending in the application.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 2 and 4-15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-54 of U.S. Patent No. 6,453,446 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims in the instant application and patent are substantial similar. They are related to an automated method for designing an IC layout in order to meet timing constraints. The patent claims anticipate the claims in the instant application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2 and 4-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsay et al. (5,461,576).

6. As to claim 2, Tsay et al. teach an automated method for designing an integrated circuit layout with a computer (summary) comprising: (a) selecting a plurality of cells that are intended to be used in the integrated circuit layout (selection of cells from cell libraries 11 at least in Fig. 3); (b) determining initial delay values associated with the cells prior to determining an initial placement of the cells (initial delay values before feed through placement shown in Fig. 3) and (c) performing an initial placement of the cells (then performing initial placement shown in Fig. 3), including determining an initial size or area of the cells in response to the initial placement (at least see Fig. 3, 6; col. 12 lines 6-14; col. 5 lines 24-67; col. 6 lines 1-67).

7. As to claim 4, Tsay et al. teach adjusting the initial delay values of the cells if necessary to meet predetermined timing constraints (at least see Fig. 2, 4, 6; summary).

8. As to claim 5, Tsay et al. teach determining a size or area of the cells that will approximately maintain the adjusted delay values (at least see Fig. 2, 4, 6; summary).

9. As to claim 6, Tsay et al. teach after determining the initial size or area of the cells, further adjusting the size or area of the cells in order to approximately maintain the initial delay values (at least see Fig. 2, 4, 6; summary).

10. As to claim 7, Tsay et al. teach routing the digital circuit to generate the integrated circuit layout using a finalized size or area of the selected plurality of cells (at least see Fig. 2, 3, 6; summary) .

11. As to claim 8, Tsay et al. teach wherein the initial delay values are determined using gain (at least see Fig. 2, 3, 6; summary).

12. As to claim 9, Tsay et al. teach wherein the initial delay values are determined using logical effort (at least see Fig. 2, 3, 6; summary).

13. As to claim 10, Tsay et al. teach wherein the initial delay values are determined by finding a preferred gain of the cells (at least see Fig. 2, 3, 6; summary).

14. As to claim 11, Tsay et al. teach wherein the preferred gain of the cells is determined using a continuous buffering assumption (at least see Fig. 2, 3, 6; summary). Note that using a buffering assumption is known to practitioners and it is inherently within the art in order to improve delay to meet all path timing constraints in an integrated circuit design.

15. As to claim 12, Tsay et al. teach wherein the initial delay values are determined during library analysis (Fig. 2, 3, 6; summary).

16. As to claim 13, wherein the initial delay values are determined using a typical load of the cells (at least see Fig. 2, 3, 6; summary).

17. As to claim 14, wherein the typical load is determined based on gain considerations (at least see Fig. 2, 3, 6; summary).

18. As to claim 15, wherein the size or area of the cells is variable and not fixed at the time the cells are selected (at least see Fig. 2, 3, 6; summary).

19. Applicants are requested to consider in their entirety the cited reference used in the rejection.

Remarks

20. Applicant's arguments filed 11/3/08 have been fully considered but they are not persuasive. Applicant argued that Tsay does not discuss the determination of size or area of cells. It is not true because Fig. 1 shows cell libraries including layout cells. Note cell libraries include information related to each cell (i.e., cell size or cell area, cell timing…). Information shown in Fig. 1 is used by placement and routing system. Fig. 5 show initial placement (software of placement tool) that selects cell from cell libraries to be placed during placement stage. Fig. 5 also show initial placement take information include net constraints and complete path constraints (these information including delays/path delays/net weight/cell delays/cell size). Fig. 5 also show refined placement (adjusting the size or area of a cell). In addition, col. 2 42-46 describes timing optimization, sizing and logic synthesis are applied (see also col. 12 lines 6-14). Slack graph is used to facilitate timing analyzer due the size of the circuit. Examiner believes that Tsay teaches the claim limitations of determining an initial size or area of the cells in respond to the initial placement. Fig. 5 also teach looping around initial placement, timing calculator, placement and refinement (placement improvement include gain determination), timing analyzer, timing constraint generator using all constraints and cell libraries shown in Fig. 1. The reference teaching sizing which is well known to artisan skill in the art. For example, sizing a cell (i.e., a buffer) that includes a combination of transistors, where each these transistors can be sizing up or down depending on design

requirement. When sizing a cell, the cell (i.e., a buffer for example) size must be known before hand. Otherwise, a designer does not know what to do if a cell size is not know. So the concept of teaching of sizing is within one skill in the art. Sizing up a cell is related to delay because it will provide more drivability capability to therefore increase speed or reduce delay to meet design requirement. The concept is known to practitioners in the art. Again concept of a continuous buffering is known to artisan skill in the art. More buffers would provide more drivability capability to reduce delay to meet design requirement. Nothing is novel that concept. The concept is well known to artisan skill in the art. Examiner respectively submits that the recited claims can't be allowed over the prior art. Nothing is novel.

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, A.U. 2825